In re Patent Application of:
SANCHES ET AL.
Serial No. **09/915,761**
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In the Specification:

Please replace the paragraph beginning at page 2, line 28, with the following rewritten paragraph:

The architecture of a processor 10 of this kind thus differs from a conventional RISC processor by its parallelism which can be found at all stages in the processing of the instructions. However, the possibilities offered by this parallelism are rarely exploited ~~to the maximum~~, and the compiled programs stored in the program memory PMEM generally comprise a large number of no-operation or NOP codes. Indeed, the conversion of a program written in a high-level language, for example the language C/C++, into a sequence of RISC type codes combined in bundles is done automatically by a compilation program that knows the structure of the processor and tries to form bundles of the largest possible size (with a maximum of four codes in the exemplary processor being described) to exploit the parallelism of the processor ~~to the maximum~~. This optimization is done by taking account of the conflicts between the codes, the availability of the execution units and the data dependence during the pipeline execution of the codes. Thus, for example, two codes designed to be executed by the same execution unit cannot be executed in parallel in the same bundle. Equally, a code using an operand that is the result of an operation that is object of another code cannot be executed so long as the code on which it depends is not itself executed.

Please replace the paragraph beginning at page 7, line 16, with the following rewritten paragraph:

The present invention also relates to a method for the reading of variable-sized instructions that may include up to N elementary instruction codes, applicable to a signal processor. The method comprises the steps of providing for a program memory comprising I individually addressable parallel-connected memory banks, with I being at least equal to N. The method further includes recording the codes of a program in the program memory in interlaced fashion, at a rate of one code per bank and per address applied to the bank. During a read cycle of an instruction, the method includes reading a sequence of codes in the I memory banks. The ~~said~~ sequence comprises the code or codes of the instruction to be read and possibly also comprises, when the number of instructions codes read is smaller than I, ~~with~~ the codes belonging to a following instruction.

Please replace the paragraph beginning at page 11, line 26, with the following rewritten paragraph:

According to the invention, these read means essentially comprise an address management circuit IAC, a code permutation circuit PCC, and a code selection circuit CSC and includes a special mode of management for the program counter PC of the processor 20 which shall be described first ~~of all~~.